{tag} {/tag}
IJCA Special Issue on International Conference on Electronics, Communication and Information systems

ICECI - Number 3

Year of Publication: 2012

Authors:
K. Mahapackialakshmi

P. Sivakumar

{bibtex}iceci1021.bib{/bibtex}

Abstract

The complexity and routability of layout depends on the number of layers, which can be used for the completion of interconnections. The global routing can be solved by graph based techniques. Efficient 3D routing methods are efficient to minimize the via overflows and total number of vias. The minimization methods rip-up and reassignment for a integer programming based layer assignment. Benchmark process is used to achieves performance of routability and minimum wire length.

Refer

ences

- Ke-Rn Dai; Wen-Hao Liu; Yih-Lang Li, "NCTU-GR: Efficient Simulated Evolution-Based Rerouting and Congestion-Relaxed Layer Assignment on 3-D Global Routing" IEEE Trans VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 20, NO. 3, MARCH 2012
- H. -Y. Chen, M. -F. Chiang, Y. -W. Chang, L. Chen, and B. Han, "Fullchip gridless routing considering double-via insertion," IEEE Trans Comput. -Aided Des. Integr. Circuits Syst. , vol. 27, no. 5, pp. 844–857,May 2008.
- C. Chu and Y. -C. Wong, "FLUTE: fast lookup table based rectilinear steiner minimal tree algorithm for VLSI design," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 27, no. 1, pp. 70–83, 2008.
- T. -C. Chen and Y. -W. Chang, "Multilevel full-chip gridless routing with applications to optical proximity correction," IEEE Trans. Comput. -Aided Des. Integr. Circuits Syst. , vol. 26, no. 6, pp. 1041–1053, Jun. 2007.
- Y. -L. Li, X. -Y. Chen, and Z. -D. Lin, "NEMO: A new implicit connection graph-based gridless router with multi-layer planes and pseudo-tile propagation," IEEE Trans. Comput. -Aided Des. Integr. Circuits Syst. , vol. 26, no. 4, pp. 705–718, Apr. 2007.

- J. A. Roy and I. L. Markov, "High-Performance Routing at the Nanometer Scale", In Proc. IEEE/ACM Intl. Conf. on Compuer-Aided Design, pp. 496- 502, Nov 2007.
- J. Cong, J. Fang, M. Xie, and Y. Zhang, "MARS—A multilevel fullchip gridless routing system," IEEE Trans. Comput. -Aided Des. Integr. Circuits Syst. , vol. 24, no. 3, pp. 382–394, Mar. 2005.
- J. Cong, J. Fang, and K. -Y. Khoo, "DUNE: A multilayer gridless routing system," IEEE Trans. Comput. -Aided Des. Integr. Circuits Syst. , vol. 20, no. 5, pp. 633–646, May 2001.
- M. Pan and C. Chu, "IPR: An integrated placement and routing algorithm," in Proc. IEEE/ACM Des. Autom. Conf. , 2007, pp. 59–62.
- ISPD 2007 Global Routing Contest and benchmark suite. http://www. sigda. org/ispd2007/rcontest
- ISPD 2008 Global Routing Contest and benchmark suite. http://www. ispd. cc/contests/ispd08rc. html

Index Terms

Computer Science Algorithms

Keywords
Global Routing Integer Programming