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Abstract

The fixed-width multiplier is attractive to many multimedia and digital signal processing systems which are desirable to maintain a fixed format and allow a little accuracy loss to output data. In this paper, we propose a new error compensation circuit in Baugh-Wooley multiplier by using the dual group minor input correction (MIC) vector to lower input correction vector compensation error. By constructing the error compensation circuit mainly from the "outer" partial products, the hardware complexity only increases slightly as the multiplier input bits increase. In the proposed 16 *16 bits fixed-width multiplier, the truncation error can be lowered by compared with the direct-truncated multiplier and the transistor count can be reduced by

compared with the full-length multiplier.

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Index Terms

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