Abstract

Networks-on-Chip (NoC) is recently proposed as an alternative to the on-chip bus to meet the increasing requirement of complex communication needs in Systems-on-Chip (SoC). Using on-chip interconnection networks in place of ad-hoc global wiring, structures the top level wires on a chip and facilitates modular design. The structured network wiring gives well-controlled electrical parameters that eliminate timing iterations and enable the use of high-performance circuits to reduce latency and increase bandwidth. Using a network to replace global wiring has
advantages of structure, performance, and modularity. With this approach, system modules (processors, memories, peripherals, etc.) communicate by sending packets to one another over the network. In NoC, nodes are arranged in the topology such that communication between any nodes is possible even though they are not directly connected. Each node is a IP core which can be a DSP, Microprocessor, Memory along with routing function which is responsible for forwarding the data packet to the neighboring node.

References

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Index Terms

Computer Science

Keywords

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