Abstract

This work describes a differential current-mode bus architecture based on driver pre-emphasis for on-chip global interconnects that achieves high-data rates while reducing bus power dissipation and improving signal delay latency. The 16-b bus core fabricated in 0.25-μm complementary metal–oxide–semi-conductor (CMOS) technology attains an aggregate signaling data rate of 64 Gb/s over 5–10-mm-long lossy interconnects. With a supply of 2.5 V, 25.5–48.7-mW power dissipation

References
Implementation of on Chip Data Bus Using Pre Emphasis Signaling

IEEE, vol. 89, no. 4, pp. 529–555, Apr. 2001

Index Terms

Computer Science

Keywords

interconnect power dessiapation delay crosstalk noise