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Abstract

This work describes a differential current-mode bus architecture based on driver pre-emphasis for on-chip global interconnects that achieves high-data rates while reducing bus power dissipation and improving signal delay latency. The 16-b bus core fabricated in 0.25- μ m complementary metal-oxide-semiconductor (CMOS) technology attains an aggregate signaling data rate of 64 Gb/s over 5–10-mm-long lossy interconnects. With a supply of 2.5 V, 25.5–48.7-mW power dissipation

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- United State Patent (Number:7557630,b2,7 july 2009) Name: sense amplifier based flip flop for reducing output delay and method thereof.

Index Terms

Computer Science

Keywords

interconnect power dessiapatation delay crosstalk noise