Abstract

Vedic multiplier is based on ancient Indian Vedic mathematics that offers simpler and hierarchical structure. Multi-valued logic results in the effective utilization of interconnections, which reduces the chip size and delay. This paper proposes that if the potential of multi-valued logic is combined with simplicity of Vedic architecture, it may result in an efficient multiplier design. Since the performance of a digital signal processor depends mainly on the multipliers used, the proposed approach can greatly enhance the performance of a digital signal...
Application of Current-Mode Multi-Valued Logic in the Design of Vedic Multiplier

References

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Index Terms

Computer Science     Signal Processing

Keywords

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