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## Abstract

The Binary logic circuits design is limited by the requirement of number of interconnections which increases the chip area with increase in logic. Multi valued logic designs are gaining importance from that perspective. Adders are one of the important part of the processing element and hence it has a focus of research. Therefore design of adders using multi valued logic can prove to be very useful. Thus there is a need to design a optimal adder. In this paper we review Quaternary Adders circuit. The proposed adders are to be design in Multi-Valued

Voltage Mode Logic and investigate the effect of one parameter on another. Optimized adders will be designed, analyzed and proposed for multi-valued logic arithmetic unit design which will achieve the practical ranges of parameters of circuit.

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### Index Terms

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### Keywords

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