Abstract

The Binary logic circuits design is limited by the requirement of number of interconnections which increases the chip area with increase in logic. Multi valued logic designs are gaining importance form that perspective. Adders are one of the important part of the processing element and hence it has a focus of research. Therefore design of adders using multi valued logic can prove to be very useful. Thus there is a need to design a optimal adder. In this paper we review Quaternary Adders circuit. The proposed adders are to be design in Multi-Valued
Voltage Mode Logic and investigate the effect of one parameter on another. Optimized adders will be designed, analyzed and proposed for multi-valued logic arithmetic unit design which will achieve the practical ranges of parameters of circuit.

References

- Elean Dubrova, "Multiple-Valued Logic in VLSI: Challenges and Opportunities" Computer 21.4,(1988),28-42
- Scott Hauck, Asynchronous design Methodologies:An Overview, Proceedings of the IEEE. Vol. 83
- Yuichi Baba, Multiple-Valued Constant-Power Adder for Cryptographic Processors, 39th International Symposium On Multiple-Valued Logic IEEE, 2009
- Hirokatsu Shirahama and Takahiro Hanyu et. al, Design of a Processing Element Based on Quaternary Differential Logic for a Multi-Core SIMD Processor, 2007 International Symposium on Multiple-Valued Logic.

Index Terms

Computer Science
VLSI

Keywords
Voltage Mode Multiple-valued Logic Quaternary Logic