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Abstract

Network on Chip (NoC) is an approach to designing the communication subsystem between IP cores in a System on a Chip (SoC). NoC improves the scalability of SoCs, and the power efficiency of complex SoCs compared to other designs. The purpose of NOC is to solve the choke point in communication and the clock problem from architecture. Each route in NOC includes some routers, and it takes a few clock periods by passing a router. When the network is in congestion, the package transmission will produce much more time delay. So adopting a appropriate routing algorithm to get the balance between the time delay and throughput rate becomes the key problem. This paper basically review of XY routing algorithm for 2D torus topology of Network on chip architecture for constant bit rate (CBR) random traffic in NIRGAM

simulator to reduce the average latency per packet and increase average throughput.

Refer

ences

- Jin-xiang Wang, Fang-fa Fu, Tian-Sheng Zhang & Yu-Ping Chen, "A Small-Granularity Solution on Fault Tolerant in 2D-Mesh Network-on-Chip", IEEE, 2010, pp. 382-384.
- Hamed S. Kia and Cristinel Ababei, "A new Fault tolerant and Congestion-aware Adaptive Routing Algorithm for Regular Networks-on-Chip", IEEE, 2011, pp. 2465-2472.
- Ruizhe Wu, Yi Wang & Dan Zhao, "A Low Cost Deadlock-free Design of Minimal-Table Rerouted XY-Routing for Irregular Wireless NOCs", 2010, Fourth ACM/IEEE International Symposium on Networks-on-Chip, pp. 199 – 206.
- Mohsen Nickray, Masood Dehyadgari & Ali Afzali-kusha, "Adaptive Routing Using Context-Aware Agents for Networks on Chips", IEEE, 2009, pp. 1-6.
- Masood Dehyadgari, Mohsen Nickray, Ali Afzali-kusha, Zainalabein Navabi, "Evaluation of Pseudo Adaptive XY Routing Using an Object Oriented Model for NOC", IEEE, 2005, pp. 204-206.
- Manas Kumar Puthal, Virendra Singh, M. S. Gaur, Vijay Laxmi, "C-Routing: An Adaptive Hierarchical NoC Routing Methodology", 2011, IEEE/IFIP 19th International Conference on VLSI and System on Chip, pp. 392 – 397.
- Shu Yan Jiang, Hao Liang, Shuo Li, Yong Le Xie, "A Test Method of Interconnection Online Detection of NoC Based on 2D Torus Topology", IEEE, 2011, pp. 183 – 187.
- Yang Quansheng, Wu Zhekai, "An Improved Mesh Topology and Its Routing Algorithm for NoC", IEEE, 2010, pp. 1-4.
- A. H. Borhani, A. Movaghar, R. G. Cole, "A New Deterministic Fault Tolerant Wormhole Routing Strategy For k-ary 2-cubes", IEEE, 2010, pp. 1 – 7.
- Xiaoqiang Yang, Huimin Du, Jungang Han, "A Node Coding and the Improved Routing Algorithm in Torus Topology", IEEE, 2008, pp. 443 – 447.
- Slavisa Jovanovic, Camel Tanougast, Serge Weber, Christophe Bobda, "A New Deadlock-Free Fault-Tolerant Routing Algorithm For NoC Interconnections", IEEE, 2009, pp. 326 – 331.
- Xiaohang Wang, Mei Yang, Yingtao Jiang, Peng Liu, "Efficient Multicasting Scheme for Irregular Mesh-Based NoCs", IEEE, 2010, pp. 384 – 387.
- Mehrdad Seyrafi, Arghavan Asad, Amir Ehsani Zonouz, Reza Berangi, Mahmood Fathy, Mohsen Soryani, "A New Low Cost Fault Tolerant Solution for Mesh based NoCs", 2010 International Conference on Electronics and Information Engineering (ICEIE 2010), pp. V2-207 - V2-213.
- Yonghui Li, HuaxiGu, "XY-Turn Model for Deadlock Free Routing in Honeycomb Networks on Chip", IEEE, 2009, pp. 900 – 903.
- Wang Zhang, Ligang Hou, Jinhui Wang, Shuqin Geng & Wuchen Wu, "Comparison Research between XY and Odd-Even Routing Algorithm of a 2-Dimension 3X3 Mesh Topology Network-on-Chip", IEEE, 2009, global congress on intelligent systems, pp. 329-333.

- Pan Hao, Hong Qil, Du Jiaqin & Pan Pan, "Comparison of 2D MESH Routing Algorithm in NOC", IEEE, 2011, pp. 791 – 795.
- Ville Rantala, Teijo Lehtonen & Juha Plosila, "Network on Chip Routing Algorithms", TUCS Technical Report No 779, August 2006.
- "A Simulator for NoC Interconnect Routing and Application Modeling", University of Southampton UK and Malaviya National Institute of Technology India, by Lavina Jain, September 1, 2007.
- Nauman Jalil, Adnan Qureshi, Furqan Khan, and Sohaib Ayyaz Qazi, "Routing Algorithms, Process Model for Quality of Services (QoS) and Architectures for Two-Dimensional 4 x 4 Mesh Topology Network-on-Chip", International Journal of Computer Theory and Engineering, Vol. 4, No. 1, February 2012, pp. 85-92.
- Yonghui Li & Huaxi Gu, "XY-Turn Model for Deadlock Free Routing in Honeycomb Networks-on-Chip", IEEE, 2009, pp. 900-903
- Shubhangi D Chawade, Mahendra A Gaikwad & Rajendra M Patrikar "Review of XY Routing Algorithm for Network-on-Chip Architecture", International Journal of Computer Applications (0975 – 8887) Volume 43– No. 21, April 2012, pp. 20-23.
- Saad Mubeen, "Evaluation of source routing for mesh topology network on chip platforms", 2009

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Index Terms

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Keywords

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