Abstract

Network on Chip (NoC) is one solution for designing communication among components in the SoC circuits with several billion transistors that will reach the market in approximately 5-10 years from now. Different topologies having various advantages according to their applications. This paper present brief idea about topologies depending on parameter.

References

- A Delay-Aware Topology-based Design for Network-on-chip Applications By Haytham


- Khalid Latif, Tiberiu Seceleeanu, Hannu Tenhunen, Power and Area Efficient Design of Network-on-Chip Router Through Utilization of Idle Buffers.


A Comparative Study of Different Topologies for Network-On-Chip Architecture


Index Terms

Computer Science
Networks

Keywords
System On Chip  Network On Chip  Different Topologies And Topology Parameter