Abstract

Poor cache memory management can have adverse impact on the overall system performance. In a Chip Multi-Core (CMP) scenario, this effect can be enhanced as every core has a private cache apart from a larger shared cache. Replacement policy plays a key role in managing cache data. So it needs to be extremely efficient in order to extract the maximum potential of the cache memory. Over the years versatile set of replacement policies have been proposed and implemented and few of them (LRU, MRU etc) have proven to work well compared to others. However recent works have shown that few counter based replacement strategies have marginally outperformed LRU for certain workloads as LRU does not dynamically adapt to changing workload patterns. This work explores three counter based replacement techniques namely Context-Based Data Pattern Exploitation (CB-DPET), Logical Cache Partitioning Technique (LCP) and Sharing and Hit-Based Prioritizing Technique (SHP). Evaluation is carried out on 4 core and 8 core platforms (apart from 2 core platform which was already done as part of previous works) using PARSEC benchmarks and various performance metrics like throughput speedup, hit rate etc are captured and compared with that of LRU. All the three methods have produced better results on the performance metrics when compared to LRU.
References


- M. Gebhart et al., Running PARSEC 2.1 on M5; University of Texas at Austin, Department of Computer Science, Technical Report, TR-09-32, Oct. 2009.

Index Terms

Computer Science

Information Sciences

Keywords

Cache Counter Throughput Hit Rate Replacement.