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Abstract

With onset of paradigms of System On Chip (SOC) to design a module for real time applications or voice codec's, The SOC's have different requirements for operands precision we propose a reusable FFT [2] using reconfigurable multiplier [6]. How ever, the FFT perform either combining N and N/2 bit multiplications in the same N bit tree multiplier. The key challenges in designing a reusable FFT are to limit the impact of flexibility on power operations that are needed for FFT butterfly to perform better than a conventional, dedicated FFT butterfly.

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Index Terms

Computer Science Integrated Circuits

Key words

System on Chip Reconfigurable reusable Butterflies