Abstract

The power consumption of a digital circuit can be reduced by decomposing it into sub circuits which can be turned off when inactive. Power can also be reduced by careful state encoding. Clock-gating techniques have been shown to be very effective in the reduction of the switching activity in sequential logic circuits. Modeling a given circuit as a finite-state machine, we formulate its decomposition into submachines as an integer linear programming (ILP) problem. A simple, but powerful state encoding method is used for the submachines to further reduce power consumption. The strategy consists in partitioning the original circuit into two structural sub circuits so that each sub circuit can be successively tested by the Computer Aided Testing (CAT) environment. In partitioning the circuit and planning the test session, the switching activity in time interval (i.e. the average power) power consumption are minimize. To minimize the average switching activity, we search for a small cluster of states with high stationary state
probability and use it to create the small sub-FSM.

Reference


Index Terms

Computer Science
Integrated Circuits

Key words

Finite-state machine
decomposition
low power
integer linear programming
system-on-chip