Abstract

Tree Multipliers are frequently used to reduce the delay of array multipliers. The objective of tree multipliers is to utilize the concept of carry save adders in reducing the partial product. Two well known tree multipliers Wallace and Dadda uses full adders and half adders for the aforesaid purpose. This paper implements a multiplier which will perform reduction of partial products using 4 bit Carry Lookahead Adders primarily instead of Full adders. This will result in fewer reduction stages as Full adders reduces 3 partial products bits to 2 giving a 1.5 to 1 ratio whereas 4 bit CLA will reduce 9 partial products bits to 5 giving 1.8 to 1 ratio. Xilinx Spartan 3E FPGA board is used for implementation of structural verilog code for the multiplier design.

References

- Pong P. Chu, FPGA Prototyping by Verilog examples: Xilinx Spartan 3 Version, John

Index Terms

Computer Science  Circuits And System

Keywords
FPGA  Multiplier  Wallace  Dadda  Carry Lookahead Adders.