Abstract

This paper presents low area and power efficient delay register using CMOS transistors. The proposed register has reduced area than the conventional register. This delay register design consist of 6 NMOS and 6 PMOS. The proposed delay register circuit has been designed in logic editor and simulated using 90nm technology. Also the layout simulation and parametric analysis of modified layout has been done. Register has been designed using full automatic layout design, semicustom layout design and fullcustom layout design. Then the results of these different designs has been observed and compared in terms of area, delay and power. The simulation results show that circuit design of delay register saves the power by 17% when designed with fullcustom and area by 61.8% when designed in semicustom.

References

Layout Design of Level Triggered Delay Register using 90 nm Technology

- Neil H. E. Weste, David Harris and Ayan Banaerjee, "CMOS VLSI design", pp. 9-10.
- Eitenne Sicard, Sonia Delmas Bendhia, Basic of CMOS Cell Design, Tata McGraw-Hill.
- Wikipedia. org/wiki/flip-flop.

Index Terms

Computer Science

Circuits And Systems
Keywords
Pass Transistor  CMOS  Power Dissipation  NMOS  PMOS