Abstract

It gives the architecture of an optimized complex matrix inversion using GAUSS-JORDAN (GJ) elimination in Verilog with single precision floating-point representation. The GJ-elimination algorithm uses a single precision floating point arithmetic components and control unit for performing necessary arithmetic operations. The proposed architecture implements the GJ-elimination algorithm for complex matrix element sequentially. Matrix inversion using GJ-elimination improves the frequency when compared with QR Decomposition algorithm. The design is targeted on XC5VLX50T Xilinx FPGA.

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Index Terms

Computer Science

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Keywords

Matrix inversion Gauss-Jordan Elimination Floating Point and True Dual Port RAM