Abstract

This paper presents design of a cache controller for 4-way set associative cache memory and analyzing the performance in terms of cache hit verses miss rates. An FSM based cache controller has been designed for a 4-way set-associative cache memory of 1K byte with block size of 16 bytes. Main memory of 4K byte has been considered. The synthesis has been performed using Xilinx Synthesis Tool (XST) with Virtex-6 FPGA device XC6VLX240T. ISim simulator is used for functional verification of the designed code. The maximum output required time i.e. hold-time after clock is 0.777ns and minimum input time before clock arrival i.e. setup-time for designed module is 1.66ns. The maximum clock frequency is 257.202MHz. The design has also been synthesized in Cadence RTL Compiler tool. Finally, ASIC implementation of the designed cache controller has been done in Cadence Encounter Digital Implementation tool and the GDSII file has been generated. The designed cache controller consumes 5.53mW of total power.


**Index Terms**

Computer Science  
Circuits and Systems

**Keywords**

Cache Memory, Main Memory, Set-Associative Cache Design, Cache Controller.