Abstract

The errors caused in the wireless communication channel are very important to identify and rectify. Viterbi Decoder is very commonly implemented technique among the various error detection and correction (EDAC) techniques. A high data-rate convolutional code suffers from decrease in the performance of bit-error-rate due to inherent drifting error between the estimated and the accurate path matric and the optimal path matric calculation during the trellis generation. The design performance is highly dependent on many factors like availability of memory elements, decoding latency of the circuit, overhead bits in the algorithm, etc. In this paper, we propose a design of Convolutional Viterbi Rate-1/3 Encoder and Decoder for a wireless communication system based on IEEE 802.11n Draft. The proposed work focuses on high data rate decoder design and simulation. The transmitter encoder and the receiver decoder are designed and simulated as separate designs for functionality verification. The purpose is to determine the feasibility to design data Error Detection And Correction (EDAC) decoder for a wireless system with multiple input multiple output (MIMO) Orthogonal Frequency Division Multiplexing (OFDM). Viterbi Encoder/Decoder combination is very effectively used in high data
rate communication systems because of its EDAC feature. The operational concept of viterbi encoding and decoding is based on Trellis coded modulation and de-modulation.

References

15. Arjit Mukherjee, “Viterbi Decoding for OFDM systems operating in narrow band
Design and Simulation of Convolutional Viterbi Decoder with Rate-1/3 for MIMO-OFDM System


Index Terms

Computer Science
Circuits and Systems

Keywords

Convolution Code, EDAC, Encoder Rate, MIMO System, OFDM.