Performance Study of Energy Recovery Logic and Conventional CMOS Full Adder

Abstract

In recent times, there is huge demand of low energy and low voltage in electronics industry. This low power dissipation is very useful in wireless operated devices and in consumer electronics market or battery operated devices. These low power circuits have ability to reduce the battery cells and reduction in these cells can enhance the uses of low weight and tiny size systems. Authors have designed the combinational circuit full adder using adiabatic method ECRL and also done comparison with traditional CMOS in this paper. The energy recovery logic ECRL is reversible logic and it can minimize the power up to 70-75. Authors have also done number of analysis on adiabatic methodology like altering the frequency and rise time and fall time of the circuit. All the results and calculations are simulated on s-edit using TANNER v.7 technology.

References

1. Richa Singh, Anjali Sharma, “Power Efficient Design Of Multiplexer Based Compressor


**Index Terms**

Computer Science

Circuits and Systems

**Keywords**

ECRL, CMOS, Full Adder. Adiabatic Logic