Abstract

In this paper different low power 8x8 bit multipliers which are implemented with Tanner Tool v13.0 at 250MHz and 500MHz frequency with 65nm technology which is having a supply voltage 1.0v. There are different CMOS multiplier circuits are analyzed which are Array multiplier, Wallace tree multiplier, Row bypass Braun multiplier, Column bypass Braun multiplier, Row and Column bypass Braun multiplier and these multiplier are realized using bridge style full adder. All these multipliers are compared in terms of delay, power dissipation and power delay product. Simulation results show that the Array multiplier and Wallace tree multiplier using bridge style adder has less power delay product and is faster as compared to other CMOS multipliers.

References

Performance Analysis of Different 8x8 Bit CMOS Multiplier using 65nm Technology


Index Terms

Computer Science  Circuits and Systems

Keywords

CMOS, PDP, VLSI, Multiplier, Array multiplier, Wallace Tree, Braun bypass multiplier.