Abstract

In this paper, Asynchronous FIR filter is designed and implemented for ECG signal processing. The use of asynchronous design approaches to construct digital signal processing (DSP) systems is a rapidly growing research area driven by a wide range of emerging energy constrained applications such as wireless sensor network, portable medical devices and brain implants. This inherent advantage of asynchronous design over conventional synchronous circuits allows them to be energy efficient. The technique used for the design and implementation is modified pipelining representation. This paper describes the analyzing and modelling of asynchronous design FIR equiripple filter using MATLAB, simulated with ISE and then implemented on FPGA devices. The proposed Asynchronous design FIR equiripple filter is implemented on two FPGA devices Xilinx’s Spartan-3E, xc3s500e-4fg320 and Virtex 2P, 2vp30ff1152-5 and compared on the basis of Asynchronous FIR and Synchronous FIR filter for hardware resource utilization as well as speed. The hardware result shows that the proposed asynchronous designed on Virtex 2P is 10.72% faster than that designed on synchronous FIR filter on given specifications. The designed FIR filter on FPGA device Virtex 2P shows efficient
FPGA based Asynchronous FIR Filter Design for ECG Signal Processing

area utilization as well as better speed as compared to that designed with synchronous FIR filter.

References


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Index Terms

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Keywords

Asynchronous FIR Filter, ECG, Filter, MATLAB, Xilinx.