Abstract

This paper presents a hardware accelerator for feature extraction based on circle views (CVs) signature suitable for shape recognition. The heavy computational and memory access needs in shape features extraction using general purpose sequential processors enforces the use of a hardware accelerator. This work presents some modifications to the original CVs signature algorithm. These modifications are intended to reduce time and space requirements for the hardware accelerator. A software version for 1NN classifier is implemented based on the modified CVs signature algorithm. This software version records 89.85% recognition rate using MPEG-7 dataset which is too close to that scored by the original CVs signature algorithm. This small reduction in performance can be ignored against the reduction in the hardware requirements and the computation time achieved. A parallel architecture for the hardware accelerator is proposed. Using 16 processing elements, the proposed hardware accelerator achieved 50.34 times speedup compared to the standard software PC implementation. A study is done to measure the effect of changing the number of processing elements on the speedup gained and the hardware components used by the proposed hardware accelerator. The
proposed hardware accelerator is implemented in a field programmable gate array (FPGA) by using Verilog hardware description language.

References


Index Terms

Computer Science

Image Processing
Keywords

Feature extraction, shape recognition, real-time image processing, hardware accelerator, FPGA.