Abstract

Orthogonal Frequency Division Multiplexing (OFDM) is a method of encoding digital data on multiple carrier frequencies. It is a specialized form of Frequency Division Multiplexing (FDM) where the carrier frequencies are orthogonal to each other. It finds applications in wideband digital communication, DSL internet access and power line communication. Fast Fourier transform (FFT) processing is one of the key procedures in popular orthogonal frequency division multiplexing (OFDM) communication systems. Structured pipeline architectures, low power consumption, high speed and reduced chip area are the primary concerns in this VLSI and signal processing domain. A 16 point FFT processor is designed using Radix-2, Radix-4 and Split-Radix algorithms and compare their performances in terms of power, delay, and Power delay product (PDP)). Vedic Multiplier and Kogge Stone adder helps in performing high speed multiplication and addition operations. The processor is implemented in RTL using Verilog HDL. Cadence environment is utilized for performing synthesis and for generating the chip layout.
References


Index Terms
Computer Science Circuits and Systems

Keywords
Radix 2, Radix 4, Split radix, Vedic Mathematics, Urdhva Triakhbhyyam, Kogge Stone Adder