

{tag} International Journal of Computer Applications  
Foundation of Computer Science (FCS), NY, USA

[Volume 168](#)

-  
[Number 6](#)

Year of Publication: 2017

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10.5120/ijca2017914469

{bibtex}2017914469.bib{/bibtex}

## Abstract

To satisfy the prerequisite of rapid speed signal processing design of high performance DSP processor is renowned. This paper represents a novel design and FPGA based pursuit of 64 bit DSP processor. The proposed design implicates multistage pipeline architecture and vedic algorithms to improve the speed. The DSP processor is rich with multiple application specific instructions (ASIP). The verilog HDL is used and the validated through extensive simulation. Synthesis results and attainment scrutiny of each systems components confirmed significant performance meliorism in the proffered DSP processor over the extant one..

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### **Index Terms**

Computer Science

Circuits and Systems

### **Keywords**

DSP Processor, Pipelining, Vedic mathematics, ASIP.