Abstract

Floating-point applications are a growing trend in the FPGA community. In nanoscale integrated circuits design as the demand for mobile computing & higher integration density is increasing power is becoming a very important constraint. Low-power is an imperative requirement for portable multimedia devices employing various signal processing algorithms and architectures. For some applications where error is in tolerable range an inexact circuit offers reduction in both static and dynamic power. In this paper, an inexact floating-point adder is designed by approximating exponent subtractor and mantissa adder. Related operations such as normalization and rounding are also dealt with in terms of inexact computing. It is then observed that it greatly reduced the power consumption and hence increased the reliability.

References


Index Terms

Computer Science Circuits and Systems

Keywords
Floating-point adders, low power, high dynamic range image, inexact circuits, error analysis.