A Review of the Design Challenges for the 3-D on Chip Network Paradigms

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Abstract

As feature sizes continue to shrink and integration densities continue to increase, interconnect delays have become a critical bottleneck in 2D NoC performance. The upcoming decades will require a change from mere transistor scaling to novel packaging architectures such as the vertical integration of chips referred as 3D integration. 3D silicon integration technologies have provided new opportunities for NoC architecture design in SoCs enabling the design of complex and highly interconnected systems in reduced space providing higher efficiency compared to 2D integration. The next challenge in front of researchers in the domain of NoC is to use NoC architecture as the backbone of the upcoming generation of 3D chips. Multiple design issues have to be addressed in this respect such as high chip temperature due to increasing power density leading to large interconnect-delays, lack of design methodologies, large area covered by vertical interconnects, problems related to optimally determining tier assignments and the placement of switches in 3D circuits. In this paper, we tried to exhibit and summarize the prevalent generic 3D NoC design issues highlighted by various recent research publications in the domain of NoC.
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References

18. J. Kim et al., “A novel dimensionally-decomposed router for on-chip communication in


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