Abstract

Digital multipliers are among the maximum essential arithmetic purposeful devices. The average performance of these systems relies upon at the throughput of the multiplier. In the meantime, the negative bias temperature instability impact occurs while a pMOS transistor is underneath negative bias (Vgs = −Vdd), increasing the threshold voltage of the pMOS transistor, and reducing multiplier pace. A similar phenomenon, positive bias temperature instability, happens when an nMOS transistor is underneath positive bias. Each effect degrade transistor pace and in the long term, the device may also fail due to timing violations. Therefore, it is essential to design dependable high-overall performance multipliers. In this paper, suggest an aging-aware multiplier model with a novel adaptive hold logic (AHL) circuit. The multiplier is able to provide higher throughput through the variable latency and may modify the AHL circuit to mitigate overall performance degradation this is because of the aging effect. Furthermore, the proposed structure can be applied to a Pre-Encoded NR4SD Multiplier.

References
1. Ing-Chao Lin, Member, IEEE, Yu-Hung Cho, and YiMing Yang, "Aging-Aware Reliable Multiplier Design With Adaptive Hold Logic" IEEE Transactions On Very Large Scale Integration (VLSI) Systems.


Index Terms

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Adaptive hold logic (AHL), Positive bias temperature instability (PBTI), Negative bias temperature instability (NBTI), Reliable multiplier