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## Abstract

This paper presents a novel hierarchical synthesis for approximating field-programmable gate array (FPGA) based adders and multipliers. Our proposed work implements the multiplier design with the following contributions: 1) providing four types of single-bit approximate adders to cover a wide range of energy-quality tradeoffs, 2) presenting many approximations of multipliers by employing the single-bit adders, 3) substituting corresponding bits of the approximate multiplier by considering the quality constrains of the results. The novel hierarchical synthesis of the approach has been integrated into our prior project, an FPGA-IoTmesh system in the field of fog computing for hardware acceleration. Combining the merits of reconfigurability of FPGAs and long-distance connection of CSRmesh technology, this work creates a diverse range of applications such as approximate designs at the network edge, as well as showing a demo for Internet-of-Things (IoT) connections covering an entire building.

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## Index Terms

Computer Science

Image Processing

## Keywords

Approximate designs, field-programmable gate array (FPGA), fog computing, Internet-of-Things (IoT)