Abstract

A low power buffer amplifier for LCD panel driving system is presented. The proposed architecture has self-biased RAIL TO RAIL complementary differential pair for full input output swing, and class B push-pull output driving stage which is suitable for large and small size liquid crystal display, compensation capacitor and resistance are used to improve the settling time and slew rate of the buffer amplifier by stabilizing phase margin, an experimental prototype is simulated using cadence specter in .35 µm CMOS technology which draws only 8 µm static current and provide a settling time of 2.8 µs and rising and 3 µs during four the act area for the design of the buffer is 49*60 µm With power supply of 3.3 it with stand with 1000 pF load capacitance the power consumption of the amplifier under static condition is 66µW.

References

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Index Terms

Computer Science

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Keywords

Rail Operational Amplifier