Abstract

Arithmetic Logic Unit plays a vital role in the central processing unit of the computer system. Addition is considered to be a primary part in the ALU. Power and speed are the major parameters to be kept in mind for designing an adder. Because of carry propagation, complexity and delay gets introduced in the adder circuit due to which addition, subtraction and multiplication obtains delay in the Arithmetic Logic unit. In order to reduce the delay, carry-free addition is introduced by QSD (Quaternary Signed Digit) Numbers. In this paper, a fast QSD Addition and Subtraction circuit is designed by use of DPG Reversible Logic Gates.

References

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**Index Terms**

Computer Science

Circuits and Systems

**Keywords**

Quaternary Signed Digit (QSD), Reversible Gate, DPG Gate, Carry Free Addition