Abstract

This paper describes the application of Imperialist Competitive Algorithm (ICA) to design and optimization of combinational logic circuits. Imperialist Competitive Algorithm is a new socio-politically motivated global search strategy that recently has been introduced for dealing with different optimization tasks. We proposed a cost function to evolve circuits at gate level
with lower number of transistors. By decreasing the total number of transistors, the area of
circuit will be optimized too. The performance of the proposed algorithm is evaluated using
different circuits from literature. The simulation results clearly demonstrate the validity of this
new technique. We can consider this heuristic algorithm as a search engine in evolutionary
hardware applications.

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Index Terms

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