Abstract

This paper describes the application of Imperialist Competitive Algorithm (ICA) to design and optimization of combinational logic circuits. Imperialist Competitive Algorithm is a new socio-politically motivated global search strategy that recently has been introduced for dealing with different optimization tasks. We proposed a cost function to evolve circuits at gate level
Evolutionary design and optimization of digital Circuits using Imperialist Competitive Algorithm

with lower number of transistors. By decreasing the total number of transistors, the area of circuit will be optimized too. The performance of the proposed algorithm is evaluated using different circuits from literature. The simulation results clearly demonstrate the validity of this new technique. We can consider this heuristic algorithm as a search engine in evolutionary hardware applications.

Reference

- M. Karnaugh, A map method for synthesis of combinational logic circuits, Transactions of the AIEE, Communications and Electronics, 72(I):593- 599, November 1953.

Index Terms

Computer Science
Digital Electronics

Key words

Combinational logic Circuit
Evolutionary Hardware
Imperialist Competitive Algorithm