Abstract

With increasing complexity of digital signal processing VLSI circuits in recent decades, design methodologies and tools have moved to higher abstraction levels. High level Synthesis has been gaining lot of interest in recent years since the major design objectives such as area, delay and power of the circuit are mutually conflicting thereby necessitating trade-offs between
different objectives. The electronic system-level (ESL) paradigm facilitates exploration, synthesis, and verification that can handle the complexity of today's system-on-chip (SoC) designs. Processor customization and High Level Synthesis have become necessary paths to efficient ESL design. This paper presents the survey of high level synthesis approaches and methodologies for simultaneous area, delay and power optimization.

Reference

- V. Krishnan and S. Katkoori, “A genetic algorithm for the design space exploration of
A Survey of High-Level Synthesis Techniques for Area, Delay and Power Optimization


Index Terms

Computer Science
Digital Circuits

Key words

High level synthesis
Design space exploration
System level design

Genetic Algorithm
Optimization
Allocation
Scheduling
Binding
Dataflow graph
Behavioral description