In this paper, the authors have compared the efficiency of the Karatsuba multiplier using polynomial multiplication with the multiplier implementing Vedic mathematics formulae (sutras), specifically the Nikhilam sutra. The multipliers have been implemented using Spartan 2 xc2s200 pq208 FPGA device having speed grade of -6. The proposed Karatsuba multiplier has been found to have better efficiency than the multipliers involving Vedic mathematics formulae.

References

- Z. Dyka and P. Langendoerfer, &quot;Area Efficient Hardware Implementation of Elliptic Curve Cryptography by Iteratively Applying Karatsuba’s Method&quot;, in Proceedings of


**Index Terms**

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**Keywords**

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