Abstract

Power has become a primary consideration during hardware design. Dynamic power can contribute up to 50% of the total power dissipation. Clock-gating is the most common RTL optimization for reducing dynamic power. Effective clock-gating implementation requires skilful application and comprehensive verification. Clock-gating support adds additional logic to the existing synchronous circuit to prune the clock tree, thus disabling the portions of the circuitry that are not in use. Here in this project designed and developed efficient data path and control units of an 8-bit microprocessor and clock gating technique applied to designed units. RTL clock-gating algorithms can be grouped into three categories: system-level, sequential and combinational. System-level clock-gating stops the clock for an entire block, effectively disabling all functionality. On the contrary, combinational and sequential clock-gating selectively suspend clocking while the block continues to produce output. In typical designs, combinational clock-gating can reduce dynamic power by about 5-to-10%. On the other hand sequential clock-gating can save significant power, typically reducing switching activity by 15-to-25% on a given block. Thus, different RTL techniques are used to reduce the power dissipation of a processor. The whole paper captured in VHDL and implemented on targeted FPGA chip and observed the power using Xilinx Xpower tool.
Design of Low Power RISC Processor by Applying Clock Gating Technique

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Index Terms

Computer Science Architecture

Keywords
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