Abstract

This article explores several hardware design methods used to implement a reconfigurable software defined radio system. The promise of software defined radios for rapidly changing the operating characteristics of radios suggests further an exciting new method to create opportunities and means for interoperability among and between any number of different radio systems. The possibilities of run-time reconfiguration techniques are explained and quantified. In this article, we are going to limit our discussion to examine the reconfigurability and low power trade-offs between: (i) building dedicated functional modules providing high performance at a high cost (Velcro approach), versus (ii) parameterizable function blocks used in
FPGA-based system development, versus (iii) dynamic partial reconfiguration which is the ability to reconfigured a portion of the FPGA while the remainder is still in operation. The main objective here is to explore and discuss the best method to design a reconfigurable, a high performance and a low power consumption software defined equipment.

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