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Abstract

There is a rapid need to explore the design issues of circuits in deep submicron nodes. This paper presents the design and performance analysis of Dual-X CCII, a widely used analog building block using state of the art Si CMOS and a proposed Hybrid (employing both CMOS and CNFET) configuration at 32nm. Current bandwidths port resistances along with power consumption have been chosen as the parameters for comparison. HSPICE simulator has been used to carry out the extensive simulations at a reduced power supply of ±0. 9V

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Index Terms

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Keywords

Dual-x Current Conveyor Si Cmos Cnt Cnfet Hybrid Configuration Bandwidth Port Resistance