Abstract

Nowadays, Multi-Processor System-on-Chip (MPSoC) have become an essential solution for embedded applications. In this paper we focus on MPSoCs using shared-memory programming model, which facilitates the programmer task. Moreover, one of the main factors affecting the performance of such systems is the management of cache coherency problem. In this context, we propose a new cache-coherency protocol. The proposed protocol is able to dynamically adapt its functioning mode according to variations in application memory access.
patterns. Experimental results show that with four cores, the new protocol reduces the number of cache misses by 77%, which results in 20% reduction in execution time and 34% decrease in the total energy consumption.

References

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Index Terms

Computer Science

Embedded Applications
Keywords
Shared-memory  Mpsoc  Cache Coherence  Performance Evaluation  Energy Consumption