Abstract

The development of conventional computing technologies faces many challenges for the last couple of decades. Power dissipation in today's computer chips becomes dominant. Reversible computing is a promising alternative to these technologies, with applications in ultra-low power, nano computing, quantum computing, low power CMOS design, optical information processing, bioinformatics etc. In reversible logic the power dissipation can be minimized or even eliminated. In this paper, the 4x4 reversible multiplier circuit is proposed with the design of new reversible gate called RAM gate. The proposed multiplier circuit is efficient compared to the existing designs in terms of gate counts, garbage outputs, constant inputs and quantum cost. The design can be generalized to construct nxn reversible multiplier circuit.

References

Design and Optimization of Reversible Multiplier Circuit


**Index Terms**

Computer Science

Integrated Circuits

**Keywords**

Reversible logic, Constant/Garbage input, Garbage output, Quantum cost

Reversible multiplier