Abstract

Nowadays mobile devices represent a significant portion of the market for embedded systems, and are continuously demanded in daily life. From the end-user perspective size, weight, features are the key quality criteria. These benchmarks criteria became the usual design constraints in the embedded systems design process and put a high impact on the power consumption. This paper survey and explore different low power design techniques for FPGA and processors. We compare, evaluate, and analyze, the power and energy consumption in three different designs namely, Altera FPGA Cyclone II which has a systolic array matrix multiplication implemented, i5 Clarkdale, and Atom Pineview-D Intel general purpose processors, which multiply two nxn 32-bit matrices and produce a 64-bit matrix as an output. We concluded that FPGA is a more power and energy efficient on low matrix size. However, general purpose processor performance is close to FPGA on larger matrix size as the larger cache size in general purpose processor help in reducing latency. We also concluded that the performance of FPGA can be improved in terms of latency if more systolic array processing elements are implemented in parallel to allow more concurrency.
References

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