Abstract

Error correction is one of the important technique for detecting and correcting errors in communication channels, memories etc. Errors are associated with all types of memories. But the NAND FLASH memories are competing in the market due to its low power, high density, cost effectiveness and design scalability. As far as the memory is concerned the testing should not consume more time. So, some DSP algorithms are used to overcome the delays by increasing the sampling rate. BCH codes are widely been used for error detection and correction. The generated check bits of the BCH encoder are appended with the message bits to form a codeword. This codeword is sent to the receiver to detect any error during the transmission. One of the main components of BCH encoder is LFSR (Linear Feedback Shift Register). LFSR find its wider application in Built-in-Self-Test, signature analyzer etc., whereas
here it is used to form parity bits to concatenate with message bits for the formation of a
codeword. The main advantage of LFSR is that it is simple to construct and it operates at very
high clock speed, but its main drawback is that the inputs are given in bit serial. To overcome
these drawbacks, DSP algorithms such as unfolding and parallel processing are used by
selecting the unfolding factor based on some design criteria. Selecting a better unfolding value
reduces the sample period, decreases the clock cycle, and increases the speed, power and the
throughput.

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Index Terms

Computer Science
Signal Processing

Keywords
Bose Chaudhuri-Hocquengham (BCH)      Cyclic Redundancy Check (CRC)
Computational Time (CT)

Galois Field (GF)

LFSR

MLC (Multi Level Cell)

unfolding

sample period reduction