Abstract

In this paper, a 12 bit Successive Approximation Analog to Digital Converter has been designed which has high resolution, less power consumption and medium speed. The circuit has been designed and simulated on Cadence tool in 0.35µm AMS technology with a supply voltage of 3.3V. Different ADC architectures are present but this SAR ADC has a salient feature of providing high resolution with increased accuracy. In this all the building blocks of SAR ADC have been designed such that they meet the desired specifications. The time domain comparator is used such as to obtain low power consumption. The layout of all the blocks has been done on Cadence Virtuoso and process corner analysis is also done to meet the desired specifications.

References

Design of 12 bit Successive Approximation Analog-to-Digital Converter


Index Terms

Computer Science Circuits And Systems

Keywords

ADC control logic sample and hold circuit analysis