Abstract

In recent years, reversible logic is the most popular and emerging technology and it will be having wide applications in the field of Low power CMOS, quantum computing and optical computing. Circuits with reversible logic gates provide low power dissipation and low energy loss. This paper proposes the Adder/Subtractor designs that are used in many DSP applications. This paper proposes the efficient Adder/Subtractor design in terms of gate count, garbage outputs, constant inputs and quantum cost. The proposed circuits will simulated using ModelSim simulator and implemented on Xilinx FPGA platform.

References
Design of Efficient Reversible Fault tolerant Adder/Subtractor

- S. Kim and VJ. Mooney, "The Sleepy keeper approach Low Power VLSI design;", Georgia Institute of Technology 2006.
Design of Efficient Reversible Fault tolerant Adder/Subtractor


Index Terms

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Keywords