Abstract

In rapid development of digital designs, memory is the most important building block, as half of the silicon area is used to store data value and program instructions. The power consumption and speed of SRAMs are important issues that have lead to multiple designs with the purpose of minimizing the power consumption. Speed and power consumption is the key parameter in ADC resolution. In this paper, we design and analyze 4-bit flash ADC by using 0.5 µm CMOS technology in Tanner Tool. In the proposed design, we are using TIQ comparator and mux based encoder for converting analog signal into digital signal, and analog input range is between 0 to 1.36V, with the supply voltage of 2.5V. Here we work on low power consumption of comparator which can be achieved by varying W/L ratio of PMOS and NMOS of TIQ comparator. The tool used for simulation purpose is S-Edit, T-Spice, W-Edit by Tanner Tool using hp0.5µm CMOS technology at supply voltage of 2.5volts.

References

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Design and Comparative Analysis of SRAM Cell Structures using 0.5 μm Technology

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Keywords

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