Abstract

An important function of any modern digital communication system is error control coding (ECC). Such coding is the field of communications that deals with techniques for detecting and correcting errors in a signal. ECC is especially useful in wireless communication systems. RS codes are the most powerful in the family of linear block codes and are arguably the most widely used type of error control codes. RS code is a type of Forward Error Correction (FEC) code and it is a non-binary, linear and cyclic block error correcting code. In this paper, the proposed work is to implement the encoder and decoder of Reed-Solomon (RS) coding scheme on the platform of VLSI using the Euclid’s algorithm. Implementation will be done on VLSI Hardware Description Language (VHDL) and the operation and results can be seen on Field Programmable Gate Array (FPGA).

References

Review of FPGA Implementation of Reed-Solomon Encoder-Decoder

- V. K. Agrawal, Gaurav Mittal, Pankaj Goel, "REVIEW OF REED SOLOMON CODE FOR ERROR DETECTION AND CORRECTION"; IJRIME JUNE-2012 Vol. 2

Index Terms

Computer Science  Circuits And Systems
Keywords

Reed-Solomon (RS)  Galois field (GF)  Generator Polynomial g(x)  Forward error Correction (FEC)

Code Rate

Block Size