Abstract

Multi-stage software router architectures permit to overcome several limitations inherent to single stage software routers. One of the key elements of the multi-stage architecture under study are the load balancers, which are used to distribute the load among backend routers. However, using a PC (Personal Computer) as a load balancer could create a performance bottleneck in the overall architecture. Since the operations performed by the load balancer are simple, we explore the possibility of an hardware-based implementation of load balancing functionality with the goal of improving its performance. In this paper, we describe the architecture of an FPGA-based load balancer and we present some performance results of its prototype implementation.
A Load Balancer for a Multi-Stage Router Architecture

References

- IETF. Forwarding and control element separation working group (ForCES). http://tools.ietf.org/wg/forces/.


**Index Terms**

Computer Science  
Networks

**Keywords**