Abstract

Timing analysis plays a vital role in chip design, which analyze whether a chip design meets the timing constraints. The main objectives of timing analysis are speed and accuracy. There are two engines for timing analysis namely Statistical Timing Analysis (STA) and Statistical Static Timing Analysis (SSTA). VLSI CAD has been gaining a lot of interest in both STA and SSTA. As technology continues to advance deeper in to the nanometer regime, a tight control on the process parameters is increasingly difficult. To account these process parameters which are probabilistic in nature while performing timing analysis SSTA is preferred. The main goal of SSTA is to improve the accuracy without any reduction in speed by considering process variations. This paper presents a survey of SSTA approaches and techniques for improving accuracy and speed by considering the topological correlations and spatial correlations.

References

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Index Terms

Computer Science

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Keywords

VLSI CAD Arrival Time Required Arrival Time Slack Critical path Conditional criticality Complementary Slack

Arrival tightness probability

Ellipse graph.