Abstract

Ensuring thermal-uniformity in an integrated circuit chip is very essential for its correct operation. Thus, in the Network-on-Chip (NoC) based system design as well, it is essential to attach cores of the application core graph to the routers in the topology graph so that thermal uniformity across the chip is maintained. However, the performance of the application should not be sacrificed to a great extent. Also, the CPU time needed to explore the overall search-space is quite high. This paper presents a tool to the designers to explore the search-space in a controlled fashion. The designer can specify the communication cost degradation that can be tolerated and the amount of effort put in to identify the potential solutions. All non-dominated solutions (in terms of communication cost and temperature variance) are reported from which the designer can choose the appropriate one for
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implementation.

References

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Index Terms

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