Abstract

As the demand of low power high performance arithmetic circuits multiplies, during this paper, we aim to introduce a style of latest MT-CMOS domino logic and FTL dynamic logic technique to style adder circuit. The MT-MOS transistors cut back the facility dissipation by minimizing sub threshold run current in the introduced domino logic circuits. The MT-NMOS semiconductor connected in discharging path of output electrical converter may be applied for pipeline structure to scale back the facility consumptions and increase fan-out. Dynamic logic vogue CMOS circuit is employed to enhance the speed and cut back the world of style by decreasing the device count. The introduced FTL dynamic logic circuit improves the performance by evaluating the computational blocks partially before its input signals are formalized and then rapidly perform a final evaluation as soon as the inputs arrive. This dynamic logic formation is like minded for an arithmetic circuit wherever the important path s created of an outsized cascade of inverting gates is created. The mixture of MT-CMOS and dynamic logic circuit provides high fan-out, high change frequencies with each lower delay and dynamic power consumption. The simulation results of those projected low power high performance circuits provide 75% power reduction, three times redoubled high speed operation and active space
reduction, whereas revealing lower sensitivity to power provide, temperature, electrical phenomenon load and method variations than the dynamic domino CMOS technologies.

References

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Performance Analysis of High Speed Domino CMOS Logic Circuits


Index Terms

Computer Science
Circuits And Systems

Keywords

CMOS  Domino Logic  FTL (Feed through Logic)  MT-CMOS  RCA