Abstract

This paper aims at reducing power and energy dissipation in Transmission Gate Logic (TGL) Multiplexer CMOS circuits comprise of reducing the power supply voltages, power supply current and delay with economical charge recovery logic. This paper designs an 8:1 Multiplexer with CMOS Transmission Gate Logic (TGL) using the Power Gating Technique, which reduces the leakage power and leakage current in active mode. Power Gating Technique uses Transmission Gate Logic (TGL) based an 8:1 multiplexer circuit which removes the degraded output. The PMOS and NMOS transistors are connected together for strong output level. Power gating technique achieves 36% reduction of leakage current and 43% reduction of leakage power in active mode, A the results of this paper are simulated on cadence virtuoso tool realized in 45nm technology with reduction of 4.021fW power, 7.381pA current and 0.7V supply voltage.
Power Optimization of 8:1 MUX using Transmission Gate Logic (TGL) with Power Gating Technique

Power Optimization of 8:1 MUX using Transmission Gate Logic (TGL) with Power Gating Technique


Index Terms

Computer Science
Circuits And Systems

Keywords
Power Gating Technique
Transistor Gate Logic (TGL)
Low Power
Leakage
Circuit