Abstract

Communication subsystems such as routers and wired or wireless network interfaces consume more power in network on chip. With the target of reduction in power consumption in network on chip, three encoding schemes are presented in this paper. These schemes work at flit level which results in reduction of self and coupling transition without making modification in the link architecture and routers. Globally to defend memories from soft error correction codes have
been used which make changes in logical value of memory cubicles without destructing the circuit. As memory expands, demand of complex decoder rises due to complex codes. One of such decoder is LDPC. We can apply these encoding schemes to linear density parity check (LDPC) codes. Power dissipation is reduced. The dynamic power value reduction is verified by using x-power analyzer tool.

References


Index Terms

Computer Science Networks
Keywords
Network On Chip  Ldpc Decoder  Switching And Coupling Activity  Encoding Scheme.