Abstract

In this paper, we designed and simulated a low power one bit, 8-bit and 32-bit full adder circuits namely Novel 10T, N14T, FA24T, CPL (complementary pass-transistor logic) and DPL (double pass-transistor logic). All the adders are tested by using one bit, 8-bit and 32-bit ripple carry adder architecture using Tanner EDA tool version 13.0. The one bit Novel 10T, N14T, XOR/XNOR function technique has been used for the generation of full adders. The proposed design successfully works with the buffering circuit in the full adder design. All full adder circuits are simulated with T-SPICE using 28nm Technology with 500 Mega Hertz frequency at 0.9 volt supply voltage. Due to lesser length requirement in the individual transistor, all the design of adders require lesser area as compared to existing design results in the tables. There is also
improvement in terms of power, delay and power-delay-product (PDP).

References


Index Terms

Computer Science

Power Electronics
Keywords
Full Adder  Ripple Carry Adder  Average Power  Delay  Power-delay-product (pdp)
Leakage Power
Noise Margin.