Abstract

Wireless base station transceiver front-end signal processing often is performed using digital
techniques. As bandwidths and IF digital-analog sampling frequencies increase, a large number of calculations are required for channelization, frequency tuning, and rate conversion. As new standards emerge, the design options are numerous for multi-protocol and multichannel transceiver front ends. The inherent flexibility of Xilinx FPGAs along with recent advances in their architectures makes them ideal for cost-efficient implementations of digital transceiver front-end functions, such as down conversions and precise channel filtering. The Xilinx development environment for digital signal processing (DSP) functions provides all of the resources needed for simultaneously developing signal processing algorithm and circuit parameters. This paper describes a design using some IP cores of Xilinx system generator and simulink software in designing the single channel to multichannel digital down converters (DDCs) for UMTS base stations. The four-channel implementations are described that efficiently map the DSP algorithms into the resources of the Virtex®-5 families of FPGAs.

References

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Index Terms

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Keywords

IF FPGA DSP DDC CDMA UMTS